9-11-00 A

UTILITY PATENT APPLICATION AND FEE TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No.	17900-27	Total Pages:	13
First Named Inventor or Application Identifier: Timothy Shuttleworth			
Express Mail Label No.	EL502386529US		

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, D.C. 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification Total Pages 10
- Descriptive title of the invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) (35 U.S.C. 113) Total Sheets 3

4. ☒ Declaration, Power of Attorney and Petition Total Pages 1

a. ☒ Not executed (copy)

b. ☐ Copy from a prior application (37 C.F.R. 1.63(d))
(for continuation/divisional with Box 17 completed)
(Note Box 5 below)

i. ☐ Deletion of Inventor(s)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(useable if Box 4b is checked)*.
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)

a. ☐ Computer readable copy

b. ☐ Paper copy (identical to computer copy)

c. ☐ Statement verifying identity of above copies

8. ☐ Assignment Papers (cover sheet & documents)

9. ☐ 37 C.F.R. 3.73(b) Statement ☐ Power of Attorney

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

14. ☐ Small Entity Statement(s) ☐ Statement filed in prior appln. Status still proper and desired.

15. ☐ Certified Copy of Priority Document(s)
(If foreign priority is claimed)

16. ☐ Other:

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information*

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No. : (fill in)

18. CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label | or ☑ New correspondence address below

OPPENHEIMER WOLFF & DONNELLY LLP
2029 Century Park East, Suite 3800
Los Angeles, California 90067 U.S.A.
Telephone (310) 788-5000 • Fax (310) 788-5100
Attn: Sung Oh

FEE CALCULATION

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	35 – 20	15 X	$ 18.00	270.00
	INDEPENDENT CLAIMS (37 CFR 1.16(b))	3 – 3	0 X	$ 78.00	0.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			$260.00	
				BASIC FEE (37 CFR 1.16(a))	$690.00
			Total of above Calculations =		
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28)				$0.00
				TOTAL =	$960.00

7. ☑ The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 16-2230:
   a. ☑ Fees required under 37 CFR 1.16.
   b. ☑ Fees required under 37 CFR 1.17.
   c. ☑ Fees required under 37 CFR 1.18.
8. ☐ A check in the amount of $960.00 is enclosed.
9. ☐ Other_____

Issuance of the official Filing Receipt at an early date is in order.

Express Mailing Label No. EL502386529US
I hereby certify that on September 8, 2000, I am depositing this correspondence and all listed attachments with the United States Postal Service "Express Mail Post Office to Addressee," service under 37 C.F.R. § 1.110, addressed to Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Joyce A. Johnson

Dated: September 8, 2000

Sung Oh, Registration No. 45,583

OPPENHEIMER WOLFF & DONNELLY LLP
2029 Century Park East, 38th Floor
Los Angeles, California 90067-3024
Telephone: (310) 788-5000
Facsimile: (310) 788-5100

PATENT APPLICATION

of

TIM SHUTTLEWORTH

for

UNITED STATES PATENT

on

SYSTEM AND METHOD FOR SYNCHRONIZING THE CLOCK FREQUENCIES OF POWER PROCESSING DEVICES AND DIGITAL SIGNAL PROCESSING DEVICES IN AN ELECTRONIC SYSTEM.

ATTORNEY DOCKET NO. 17900-27

SHEETS OF DRAWINGS:

OPPENHEIMER WOLFF & DONNELLY LLP
Att'n: Sung Oh
2029 Century Park East, 38th Floor
Los Angeles, California 90067-3024
(310) 788-5000

Inventor:

Timothy Shuttleworth
Los Angeles, California

SYSTEM AND METHOD FOR SYNCHRONIZINGTHE CLOCK FREQUENCIES OF POWER PROCESSING DEVICES AND DIGITAL SIGNAL PROCESSING DEVICES IN AN ELECTRONIC SYSTEM.

BACKGROUND OF THE INVENTION

1. Field of Invention

This invention relates generally to a system and method for synchronizing the clock frequencies of power processing devices and digital signal processing devices in an electronic system.

2. Background of the Invention

Power amplifiers and power supplies based upon linear circuit technology have been traditionally inefficient and relatively heavy. Enormous heatsinks, fans, and other cooling methods are usually required to dissipate the power loss while having the undesirable effect of adding to the overall weight of a system.

In recent years, high frequency switching circuit technology, where the switching is based upon some clock with a predetermined frequency, has gained rapid and sophisticated development. Particularly, switching circuits have been developed to use pulse width modulation (PWM) to carry signals and deliver power. The design advantage of a PWM power supply is that small components can be used to rectify and smooth the high-frequency alternating current. The design advantage of a PWM amplifier is that the output devices in a PWM amplifier are unbiased and switch completely off at each half-wave cycle. One of the advantages is that these power supplies and amplifiers are inherently more efficient and run cooler than traditional linear circuit amplifiers and power supplies. A further advantage is that power processing with switching circuits can be accomplished with much less mass than traditional linear power processing circuits.

Electronic systems which employ power supplies and power amplifiers may also employ Digital Signal Processors (DSP) for various types of processing. These processors are also based upon some clock with a predetermined frequency. If the power supply and power amplifier are both pulse width modulated, a problem will likely exist if the Digital Signal Processor's clock is out of sync with the clock on any of the power processing devices. Namely, the difference or sum in clock frequency and/or clock synchronization may generate noticeable noise or induce a difference frequency. In the

case of an audio system that employs PWM power processing and Digital Signal Processing, this may translate to audible tones.

Therefore, a need exists for a system and method for synchronizing the clocks of the power processing devices and digital signal processing devices in electronic systems.

3. SUMMARY OF THE INVENTION

A general feature of the present invention is to provide a system and method for synchronizing the clock of the power processing devices and digital signal processing devices in an audio system. Of course, it is not necessary to the invention that the system be an audio system, rather, any system employing PWM power processing devices where the clocks of those device(s) need to be in sync with the clock of another device such as a digital signal processor may be used.

In one embodiment of the present invention, the system may include a clock, a digital signal processor (DSP), and a pulse width modulated (PWM) power processing device wherein the digital signal processor and the power processing device would use the clock for their operation. The DSP and the PWM power processing device may use, for operation, the frequency of the clock, or a multiple, integer fraction thereof, such that all clocks are synchronized and all potential sum and/or difference frequencies are predetermined and fall outside the audible frequency range.

In another embodiment of the present invention, the system may include a sensor capable of detecting and reporting the clock information either through a metal wire, fiber optic wire, infrared or radio frequency link, which can allow the power processing devices to use the same clock as the DSP.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an exemplary system diagram in accordance with one embodiment of the present invention, in which a digital signal processor and a pulse width modulated power supply and a pulse width modulated power amplifier use the same clock or integer related derivative of the clock so that all devices based upon the clock are running synchronously.

FIG. 2 is an exemplary system diagram in accordance with one embodiment of the present invention, in which a digital signal processor and a pulse width modulated power supply and a pulse width modulated power amplifier use the clock inside the digital signal processor or integer related derivative of the clock so that all devices based upon a clock are running synchronously.

FIG. 3 is an exemplary system diagram in accordance with one embodiment of the present invention, in which a digital signal processor and a pulse width modulated power supply and a pulse width modulated power amplifier derive their clock frequencies from the clock inside the digital signal processor via an electromagnetic communication link so that all devices based upon a clock are running synchronously.

DETAILED DESCRIPTION OF THE INVENTION

This description is not to be taken in a limiting sense, but is made merely for the purpose of illustrating the general principles of the invention. The section titles and overall organization of the present detailed description are for the purpose of convenience only and are not intended to limit the present invention. Accordingly, the invention will be described with respect to synchronizing clock frequencies in an audio system. It is to be understood that the particular system described herein is for illustration only; the invention also applies to other systems employing PWM (pulse width modulation) power processing devices and Digital Signal Processing devices.

I. SYNCHRONIZING THE DIGITAL SIGNAL PROCESSOR AND POWER PROCESSING DEVICES

FIG. 1, illustrates by way of example a simplified system diagram representing one embodiment of the present invention, wherein a PWM power amplifier 1 and a PWM power supply 2 and a DSP 3 use a common clock 30 for their operation.

The design of PWM power amplifiers and power sources is well appreciated in the art and it follows that there are various methods and design choices involved in their construction. However, all pulse width modulation power processing devices will contain a switching controller (4, 5) and/or a switching circuit (7, 8).

At its fundamental level, the PWM power amplifier 1 uses a switching controller 4 and a switching circuit 7 to amplify an audio signal. The switching controller 4 tells

the switching circuit when to turn off and on based upon the audio input signal and a clock with a predetermined frequency which results in the creation of a frequency square wave carrier modulated by the audio signal. The amplitude of this modulated signal is constant and determined by the control voltage (24) of the switching circuit 7. Varying the control voltage (24) in turn varies the amplification of the audio signal.

At its fundamental level, the PWM power supply 2, uses a switching controller 5 and switching circuit 8 to convert incoming power to higher frequency pulses by turning the switching circuit on and off, based upon a clock with a predetermined frequency, while at the same time regulating the power by pulse width modulation. Simply, the duration of each power pulse is varied in response to the needs of the circuitry being supplied. The switch controller 5 controls the width of the pulses by turning on and off the switching circuit 8 at a certain rate. Finally, a transformer reduces the switched pulses' voltage to the level required by the circuits and, by rectification and filtering 18, turns it into pure direct current.

The digital signal processor 6 takes as input a signal 15, and through various algorithms digitally processes the signal for an intended result. The fundamental operation of a digital signal processor is based upon a clock with a predetermined frequency.

Each electronic component; namely, the PWM power supply, the PWM power amplifier, and the DSP use the clock 30 for their operation. The frequency of the clock, for example, may be 96 kHz because it is an industry standard as a clock frequency for DSP's. However, other frequencies may be used such as 44.1 kHz to 48 kHz and 88.2 kHz. Each component receives the clock signal at a clock signal input (9, 10, 29) via a clock signal link (22, 21, 28). The clock signal link may be a wire link, a fiber optic link, or an electromagnetic link. Each component may use the actual frequency being generated by the clock 30, or a multiple, or integer fraction thereof, such that all of the components (1, 2 and 3) are synchronized and all potential sum and/or difference frequencies may be predetermined and fall outside the audible frequency range. For example, the DSP may run at 96 kHz or 48 kHz, while the PWM power amplifier may run at 192 kHz.

FIG. 2, illustrates by way of example a simplified system diagram representing a further embodiment of the present invention, wherein a PWM (pulse width modulated) power amplifier 1 and a PWM power supply 2 derive their clock frequencies from the clock 6 inside the Digital Signal Processor 2.

As discussed above, all three electrical components (1,2 and 3) use the same clock for their operation. However, within this embodiment, the clock 6 is located inside the DSP 3. The clock frequency of the Digital Signal Processor is fixed to a predetermined industry standard, whereas in PWM power processing devices, the clock frequency may be fixed to an arbitrary number within a predetermined range. Therefore, in this embodiment all electrical components use the clock inside the DSP.

The power supply 3 supplies the power for the power amplifier 1 at the power input 12 and supplies the power for the digital signal processor 3 at the power input 11. The clock 6 in the digital signal processor 1 is also used by the PWM power amplifier 1 and the PWM power supply 2 so as to synchronize the power processing devices with the digital signal processor. The clock signal is received in the PWM power amplifier and the PWM power supply at the clock inputs 9 and 10 respectively. The connection lines 22 and 21 connecting the clock 6 in the digital signal processor 3 with the clock inputs 9 and 10 respectively may be wire connection or a fiber optic connection. Alternatively, as shown in **FIG 3**, the connection may be an electromagnetic wireless connection, where the digital signal processor transmits the clock signal via an electromagnetic transmitter 9 and the PWM power processing devices (1 and 2) receive the clock signals at their clock inputs which are electromagnetic receivers (9 and 10 respectively).

In closing, it is noted that specific illustrative embodiments of the invention have been disclosed hereinabove. However, it is to be understood that the invention is not limited to these specific embodiments. With respect to the claims, it is applicant's intention that the claims not be interpreted in accordance with the sixth paragraph of 35 U.S.C. § 112 unless the term "means" is used followed by a functional statement.

WHAT IS CLAIMED IS:

1. A system for synchronizing the clock frequencies of power processing devices and digital signal processing devices in an electronic system comprising :

a clock;

a pulse width modulated power processing device; and

a digital signal processor;

wherein said pulse width modulated power processing device is communicatively coupled to said clock;

wherein said digital signal processor is communicatively coupled to said clock;

wherein said pulse width modulated power processing device and said digital signal processor use said clock for their operational clock frequencies.

2. A system according to claim 1, wherein the power processing device is a pulse width modulated power amplifier.

3. A system according to claim 1, wherein the power processing device includes a pulse width modulated power supply.

4. A system according to claim 3, wherein the power processing device provides power to the digital signal processor.

5. A system according to claim 3 wherein the power processing device further includes a pulse width modulated power amplifier.

6. A system according to claim 5 wherein the pulse width modulated power supply provides power to the pulse width modulated power amplifier and the digital signal processor.

7. A system according to claim 1 wherein the clock operates at 96kHz.

8. A system according to claim 5, wherein the pulse width modulated power amplifier drives a loudspeaker.

9. A system according to claim 1, wherein the clock has a clock frequency that is used by the digital signal processor.

10. A system according to claim 9, wherein the digital signal processor uses a multiple of the clock frequency for its operation.

11. A system according to claim 9, wherein the digital signal processor uses an integer fraction of the clock frequency for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

12. A system according to claim 9, wherein the digital signal processor uses integer related derivatives of the clock frequency for its operation.

13. A system according to claim 1, wherein the clock has a clock frequency that is used by the pulse width modulated power processing device.

14. A system according to claim 13, wherein the pulse width modulated power processing device uses a multiple of the clock frequency for its operation.

15. A system according to claim 13, wherein the pulse width modulated power processing device uses an integer fraction of the clock frequency for its operation.

16. A system according to claim 13, wherein the pulse width modulated power processing device uses integer related derivatives of the clock frequency for its operation so that the sum and difference frequencies fall outside of the audible frequency range.

17. A system for synchronizing the clock frequencies of power processing devices and digital signal processing devices in an electronic system comprising :

a pulse width modulated power supply;

a pulse width modulated power amplifier; and

a digital signal processor, including:

a clock;

wherein said pulse width modulated power supply is communicatively coupled to said clock in said digital signal processor;

wherein said pulse width modulated power amplifier is communicatively coupled to said clock in said digital signal processor;

wherein said digital signal processor and said pulse width modulated power supply and said pulse width modulated power amplifier use said clock in said digital signal processor for its operational clock frequency.

18. A system according to claim 17, wherein the pulse width modulated power supply provides power to the pulse width modulated power amplifier and the digital signal processor.

19. A system according to claim 17, wherein the clock in said digital signal processor operates at 96 kHz.

20. A system according to claim 17, wherein the pulse width modulated power amplifier drives a loudspeaker.

21. A method for synchronizing the clock frequencies of power processing devices and digital signal processing devices comprising the steps of:

using a clock to operate a digital signal processor (DSP); and

using the clock to operate a pulse width modulated (PWM) power processing device.

22. A method according to claim 21, wherein the clock is within the DSP.

23. A method according to claim 21, wherein the PWM power processing device is a PWM power amplifier.

24. A method according to claim 21, wherein the PWM power processing device is a PWM power supply.

25. A method according to claim 24, wherein the PWM power supply provides power to the DSP and to a PWM power amplifier.

26. A method according to claim 21, wherein:

the DSP has an input and an output; and

the PWM power supply processing device has an input and an output.

27. A method according to claim 26, wherein the output of the DSP feeds the input of the PWM power supply.

28. A method according to claim 26, wherein the output of the PWM power supply feeds the power input of the DSP.

29. A method according to claim 23, wherein the PWM power amplifier drives a loudspeaker.

30. A method according to claim 23, wherein the PWM power amplifier drives a computer.

31. A method according to claim 21, wherein the clock has a clock frequency that is used by the DSP.

32. A method according to claim 21, wherein the clock has clock frequency that is used by the PWM power processing device.

33. A method according to claim 32, wherein the PWM power processing uses a multiple of the clock frequency for its operation.

34. A method according to claim 31, wherein the DSP uses a multiple of the clock frequency for its operation.

35. A method according to claim 21, wherein the clock operates at 96 kHz.

ABSTRACT

The present invention synchronizes the clock of the power processing devices and digital signal processing devices in an audio system. The system may include a clock, a digital signal processor (DSP), and a pulse width modulated (PWM) power processing device wherein the digital signal processor and the power processing device would use the clock for their operation. The DSP and the PWM power processing device may use, for operation, the frequency of the clock, or a multiple, integer fraction thereof, such that all clocks are synchronized and all potential sum and/or difference frequencies are predetermined and fall outside the audible frequency range. The may also include a sensor capable of detecting and reporting the clock information either through a metal wire, fiber optic wire, infrared or radio frequency link, which can allow the power processing devices to use the same clock as the DSP.

Figure 1

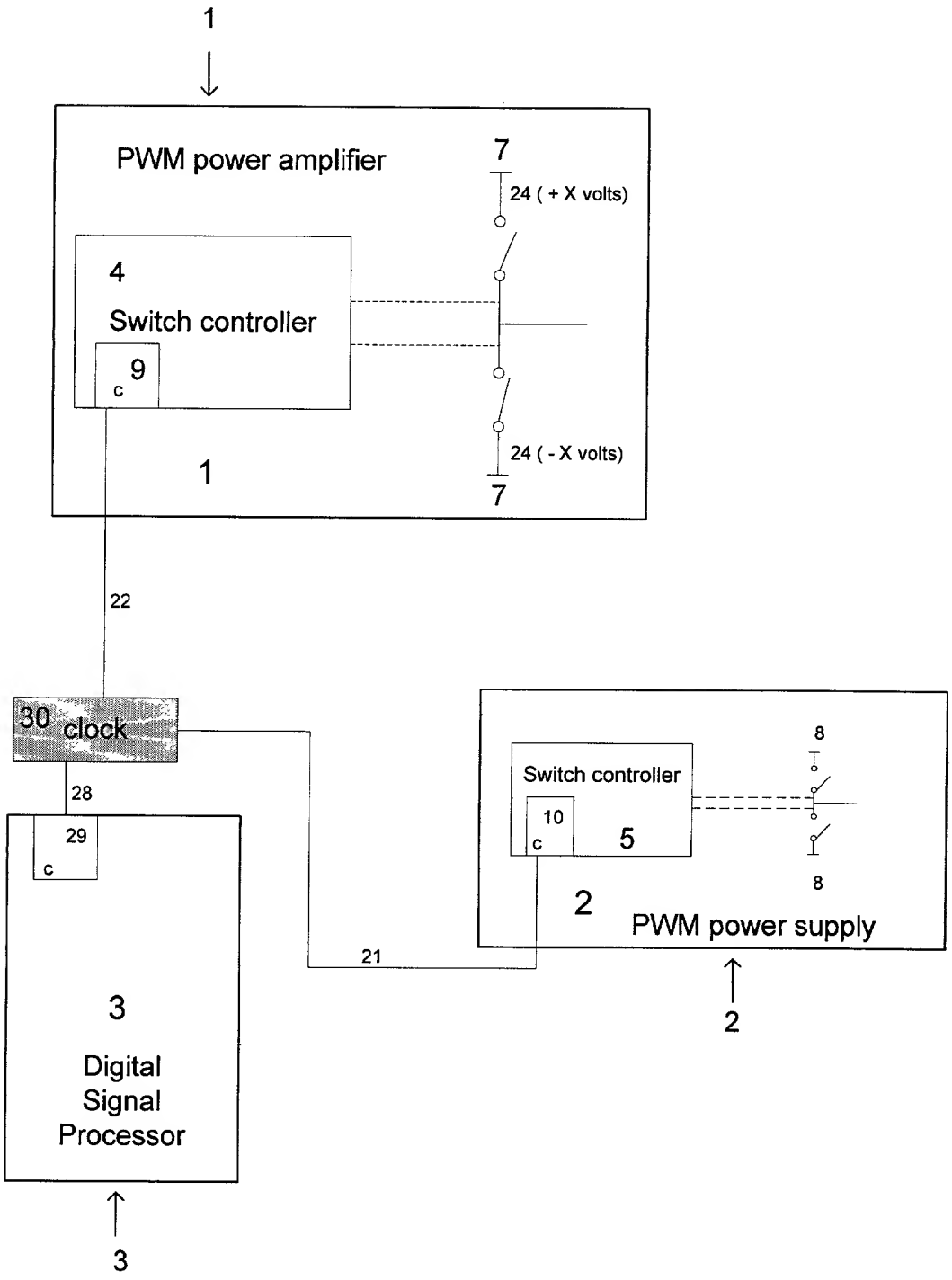

1
PWM power amplifier
7
24 (+ X volts)
4
Switch controller
9
c
1
24 (- X volts)
7
22
30 clock
28
29
c
3
Digital
Signal
Processor
3
Switch controller
10
c
5
8
8
2
PWM power supply
21
2

Figure 2

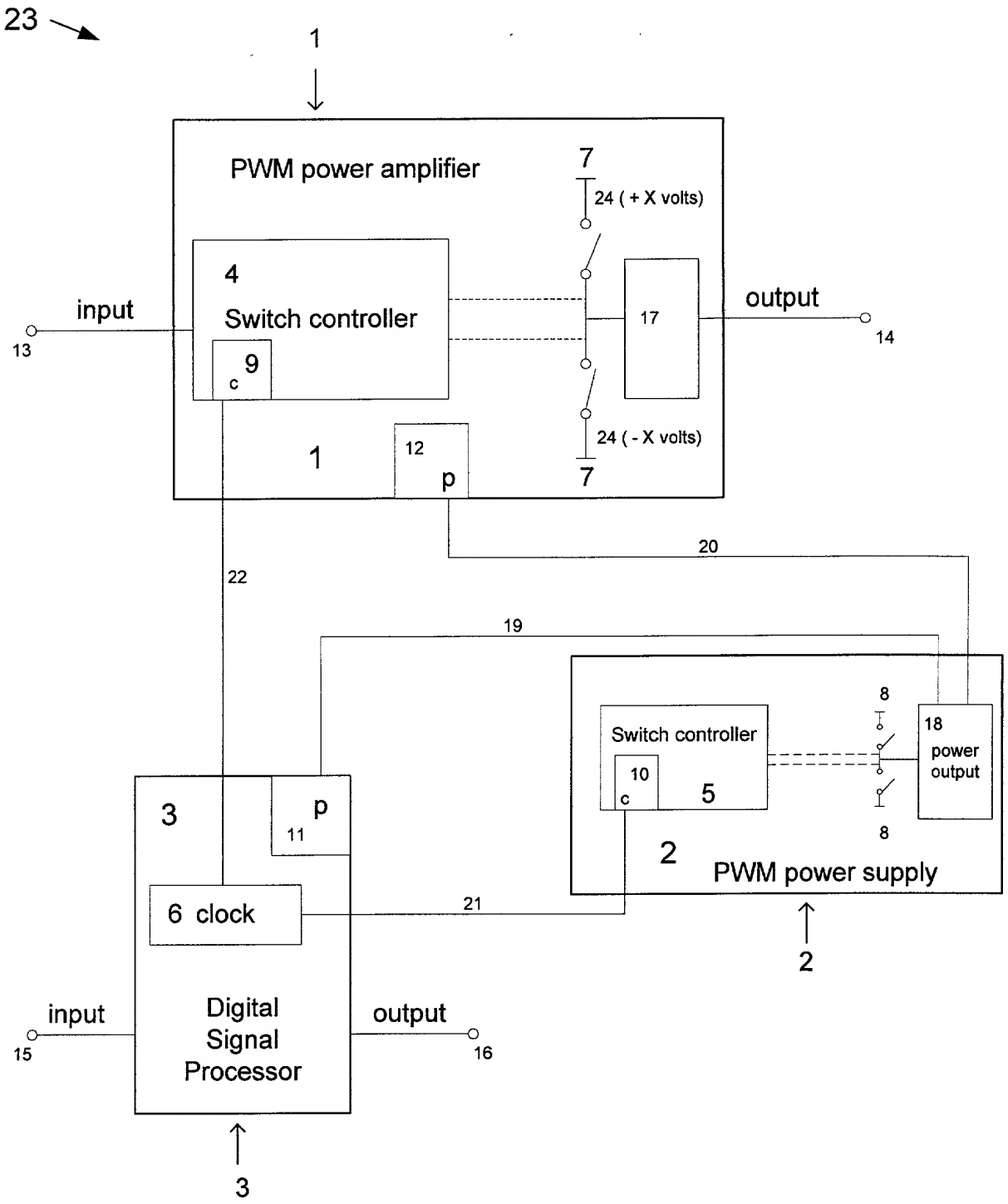
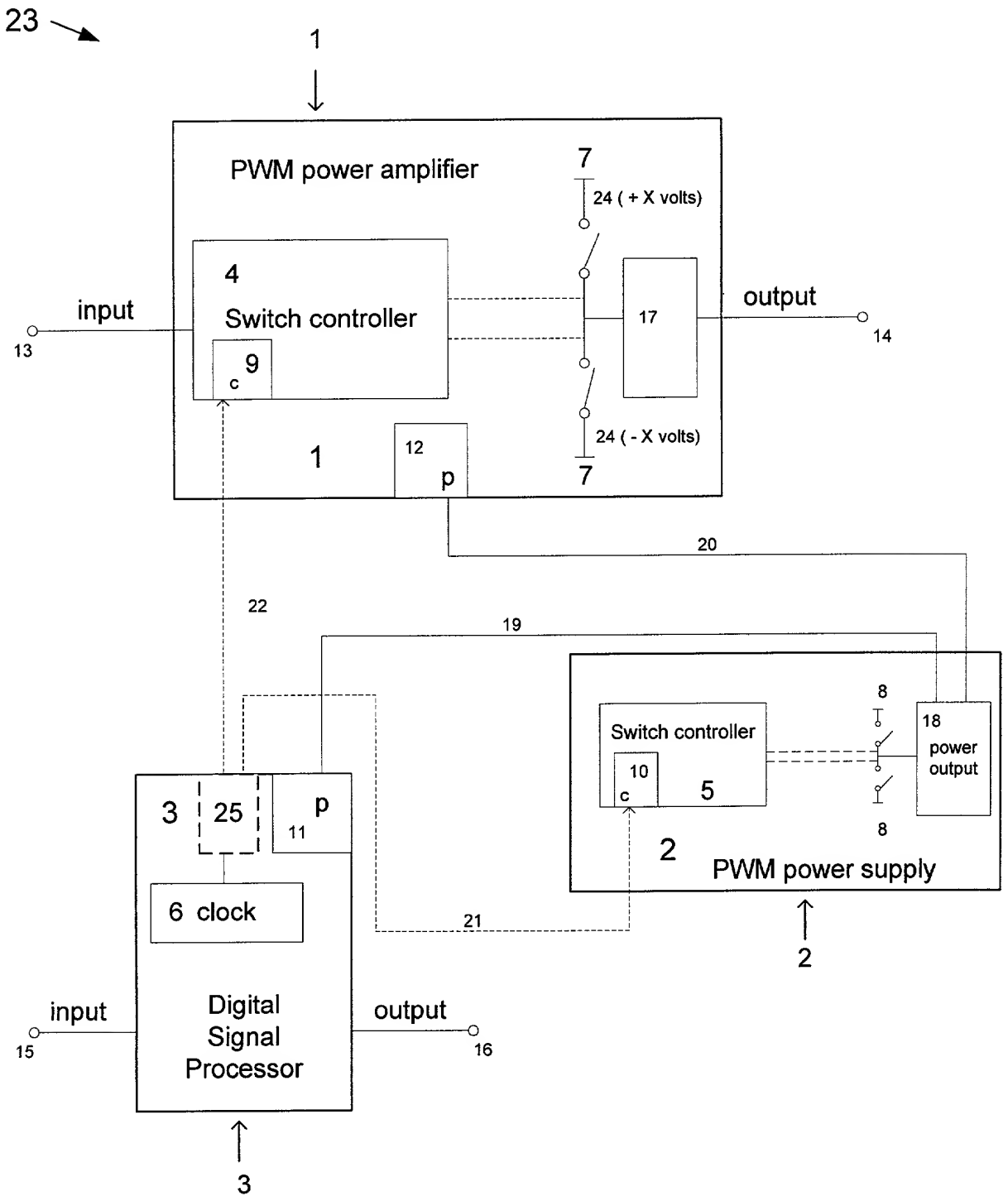

23
1
PWM power amplifier
7
24 (+ X volts)
4
Switch controller
9
c
input
13
17
output
14
24 (- X volts)
7
1
12
p
20
22
19
8
Switch controller
10
c
5
18
power
output
8
2
PWM power supply
3
p
11
6 clock
21
2
input
15
Digital
Signal
Processor
output
16
3

Figure 3


23
1
PWM power amplifier
7
24 (+ X volts)
4
Switch controller
9
c
input
13
17
output
14
24 (- X volts)
7
1
12
p
20
22
19
8
Switch controller
10
c
5
18
power
output
8
2
PWM power supply
3
25
p
11
6 clock
21
2
input
15
Digital
Signal
Processor
output
16
3

Docket No. 17900-27

DECLARATION AND PETITION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled SYSTEM AND METHOD FOR SYNCHRONIZING THE CLOCK FREQUENCIES OF POWER PROCESSING DEVICES AND DIGITAL SIGNAL PROCESSING DEVICES IN AN ELECTRONIC SYSTEM, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application of which priority is claimed.

Prior Foreign Application(s)

Priority Claimed

(Number)(Country)(Day, month, year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	Filing Date	(Status: Patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please send all correspondence to:
OPPENHEIMER WOLFF & DONNELLY LLP
2029 Century Park East, Suite 3800
Los Angeles, California 90067
Attn: Sung Oh
(310) 788-5000

Wherefore I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, and this petition.

Full name of sole or first inventor: Timothy SHUTTLEWORTH

INVENTOR'S SIGNATURE_____ DATE_____

Residence: 5102 Calatrana Drive, Woodland Hills, California 91364
Citizenship: U.K.
Post Office Address: Same as above